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EXAMINER

VIEAUX, GARY

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/892,506

Applicant(s)

MURAYAMA ET AL.

Examiner

Gary C. Vieaux

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 27 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Amendment***

The Amendment filed May 20, 2005 has been received and made of record. In response to the first Office Action, claims 1, 5, 8, and 12 have been amended, claim 2  
5 has been cancelled, and claim 17 has been added.

### ***Response to Amendments***

In response to Applicant's amended claims 1 and 8, the Examiner finds the amendments directly address and correct the previous informalities. Therefore, the  
10 objections to claims 1 and 8 are hereby withdrawn.

In response to Applicant's amended claims 5 and 12, the Examiner finds the amendments to claims 5 and 12 do not cure the 35 U.S.C. §112, second paragraph, rejection, as they continue to fail to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The amended language "as viewed  
15 from above" does not clearly delineate the subject matter which applicant regards as the invention.

### ***Response to Arguments***

Applicant's arguments filed May 27, 2005, have been fully considered but they  
20 are not persuasive.

Regarding independent claims 1 and 8, Applicants submit that the cited combination fails to disclose or suggest each and every feature of the invention as

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claimed, with the missing claim limitation being "each of said bonding pads having an exposed surface" (Remarks, p. 9-10.) The Examiner respectfully disagrees.

In support of their position, Applicants cite the Hatta reference as "allegedly disclosing a light shielding plate having an opening such that 'no light is incident other than on the image area of the chip'. See Hatta at col. 4, line 47-48" (Remarks, p. 9.)  
The Examiner agrees with the Applicants that the light shielding plate 17 of the Hatta reference is arranged so that "no light is incident other than on the image area 21 on the chip 14" in order to reduce stray light (col. 4 lines 43-50.) However the language of claims 1 and 8, as currently written, only calls for the bonding pads "having an exposed surface" and does not include limitations relating to exposure to light emitted via the light suppressing layer (light shielding plate 17.) In addition to the Applicant Admitted Prior Art (AAPA) providing the limitation of the "bonding pads having an exposed surface" citing the AAPA "Each of the bonding pads for external connection has an exposed surface" (p.3 lines 10-11), further review of the Hatta reference additionally provides bonding pads which include exposed surfaces in which bonding pads 15 are connected with wire 19 (figs. 2 and 5; col. 3 lines 42-45; and figs. 16 and 17), without providing a teaching away from or a contradiction to such a combined configuration. Therefore, based on the current language of claims 1 and 8, and in light of both the AAPA and the Hatta reference providing the claimed limitation, the Examiner respectfully stands behind the 35 U.S.C. §103(a) rejection.

Applicants further submit that combining the light shielding plate 17 of Hatta with the linear image sensor chip would render the device unfit for its intended purpose, and

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is therefore an inappropriate modification (Remarks, p. 10.) However, based on the foregoing, particularly taking into consideration of the claims as currently written and that the Hatta reference is not rendered unsatisfactory for its intended purpose with its bonding pads having exposed surfaces, as well as there being no indication that the device would not function given this configuration, the Examiner respectfully disagrees and again, stands behind the 35 U.S.C. §103(a) rejection as being proper.

Finally, in response to applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, motivation is provide by knowledge generally available to one of ordinary skill in the art (Office Action of March 24, 2005, p. 4 lines 9-15), motivation which is also supported by the Hatta reference (col. 4 lines 43-50.)

Regarding claims 3-7 and 9-16, each depend either directly from or indirectly from independent claims 1 and 8, and thus inherit all the limitations of independent claim 1 and 8, respectively. Consequently, based on their dependence and the foregoing response to arguments relating to claims 1 and 8, the Examiner respectfully upholds the 35 U.S.C. § 103(a) rejections to claims 3-7 and 9-16.

***Claim Rejections***

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

5       The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**Claims 5, 12, and 17** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The language "as viewed from above" does  
10       not clearly delineate the subject matter which applicant regards as the invention. Furthermore, this language is considered vague and indefinite, as there is no definitive point of reference or relation given regarding either the apparatus or the vantage point of viewing. These claims will be directly addressed on their merits as best interpreted/understood by the examiner.

15

***Claim Rejections - 35 USC § 103***

      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

20       (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

25       **Claims 1, 4, 5, 8, 11, 12, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hatta (US 5,087,964), in view of Masuda et al. (US 5,249,055), in view of Examiner's Official Notice.

Regarding claim 1, Applicant, in the Background of the Invention, discloses a linear image sensor chip comprising a semiconductor substrate having an elongated shape (p. 1 line 20), an image pickup section formed on said semiconductor substrate (p. 1 lines 20-21), said image pickup section including (i) at least one photodiode group  
5 composed of a plurality of photodiodes formed in one surface of said semiconductor substrate along a longitudinal direction of said semiconductor substrate (p. 2 lines 7-9) and (ii) a charge transfer element provided for each said photodiode group (p. 1 lines 23-24), a peripheral circuit section (p. 3 lines 3-5), a plurality of bonding pads formed on the surface of said semiconductor substrate outer than said at least one photodiode  
10 group with respect to the longitudinal direction, each of said bonding pads having an exposed surface (p. 3 lines 6-11), a light-suppressing layer formed above said semiconductor substrate and covering a peripheral area (p.3 lines 16-17), and bonding wires connecting the bonding pads with lead electrodes (p.3 lines 18-21.)

The AAPA is not found to explicitly disclose the light-suppressing layer covering  
15 a peripheral area of each said photodiode, the peripheral circuit section being formed on said semiconductor substrate and disposed outer than said image pickup section with respect to the longitudinal direction, or a plurality of metal lines formed on the surface of said semiconductor substrate, each of said metal lines having an end connected to one of said bonding pad and another end connected to said peripheral circuit or said charge  
20 transfer element.

Nevertheless, Hatta teaches a light-suppressing layer which only allows light to pass through to an image area (fig. 1 and 2 indicator 7; col. 1 lines 24-33.) It would

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have been obvious to one of ordinary skill in the art at the time of the invention to include the light-suppressing layer to cover everywhere but where the light strikes the image area as taught by Hatta, with photodiodes of the image sensor as taught by the AAPA, in order to ensure the only light intended to strike the photodiode reaches the photodiode, as well as to prevent light from radiating to a part other than the imaging area.

Further, it is well known in the art to provide a peripheral circuit section formed on a semiconductor substrate and disposed outer than an image pickup section with respect to the longitudinal direction as demonstrated by Masuda (figs. 10 and 4a indicator 7.) It would have been obvious to one of ordinary skill in the art at the time of the invention to include circuitry peripheral to the photodiodes (figs. 10 and 4a indicator 4) and the charge transfer elements (figs. 10 and 4a indicator 5) as taught by Masuda, with the image sensor as taught by Hatta and the AAPA in order to minimize the width of the image sensor chip, resulting in a more compact image sensor, which is particularly important in full-page-width imaging.

Official Notice is taken regarding the etching of metal lines on a semiconductor substrate for the purposes of forming bonding pads, interconnects and trace runs; a practice that is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention for the image sensor as taught by Hatta, Masuda and the AAPA to include a plurality of metal lines formed on the surface of said semiconductor substrate, each of said metal lines having an end connected to one of said bonding pad and another end connected to the circuitry peripheral to the



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photodiodes in order to be able to pass signal from the photodiodes to the bonding pads and eventually to circuitry external to the semiconductor substrate for additional processing, such as to a printing apparatus, an image memory or an image display device.

5        Regarding claim 4, the AAPA, Hatta, Masuda, and Examiner' Official Notice teach all the limitations of claim 4 (see the 103(a) rejection to claim 1 supra) including teaching an image sensor chip wherein said light-suppressing layer covers also said peripheral circuit section (figs. 1-3 indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents light from radiating to a part other than the imaging  
10    area.)

Regarding claim 5, the AAPA, Hatta, Masuda, and Examiner' Official Notice teach all the limitations of claim 5 (see the 103(a) rejection to claim 1 supra) including teaching an image sensor chip wherein said light-suppressing layer covers said metal lines at least in a region sideward along said at least one photodiode group (figs. 1-3  
15    indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents light from radiating to a part other than the imaging area.)

Regarding claim 8, Applicant, in the Background of the Invention, discloses a linear image sensor comprising a package including a bottom portion, sidewall portions and a lid portion (p. 3 lines 13-17), and a plurality of lead electrodes, passing through  
20    said sidewall portions, and reaching an external space (p. 3 lines 18-19), said bottom portion and said sidewall portions being made of light shielding material (p.3 lines 14-15) and said lid portion having a window made of transparent material (p. 3 line 15), a

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linear image sensor chip fixed in the inner space of said package (p. 3 line 13), said linear image sensor chip including (1) a semiconductor substrate (p. 1 line 20) having an elongated shape along a direction generally coincident with the longitudinal direction (p.2 lines 7-9), (2) an image pickup section formed on said semiconductor substrate, said image pickup section including (i) at least one photodiode group composed of a plurality of photodiodes formed in one surface of said semiconductor substrate along a longitudinal direction of said semiconductor substrate (p. 2 lines 7-9) and (ii) a charge transfer element provided for each said photodiode group (p. 1 line 23-24), (3) a peripheral circuit section (p. 3 line 3-5), (4) a plurality of bonding pads formed on the surface of said semiconductor substrate outer than said at least one photodiode group with respect to the longitudinal direction of said semiconductor substrate, each of said bonding pads having an exposed surface (p. 3 lines 6-11), a light-suppressing layer formed above said semiconductor substrate and covering a peripheral area (p.3 lines 16-17), and a plurality of bonding wires each electrically connecting one of said lead electrodes to a predetermined one of said bonding pads (p. 3 lines 18-21.)

The AAPA is not found to explicitly disclose a package defining an elongated inner space, the lead electrodes extending from an end region of the elongated inner space, the lid portion having an elongated window, the semiconductor substrate being generally coincident with the longitudinal direction of said bottom portion, the peripheral circuit section formed on the semiconductor substrate and disposed outer than said image pickup section with respect to the longitudinal direction of said semiconductor substrate, a plurality of metal lines formed on the surface of the semiconductor

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substrate, each of the metal lines having an end connected to one of the bonding pads and another end connected to the peripheral circuit or the charge transfer element, and a light-suppressing layer formed above the semiconductor substrate and covering a peripheral area of each said photodiode.

5            Nevertheless, Hatta is found to teach a package defining an elongated inner space (fig. 3), the lid portion having an elongated window (fig. 3 indicator 22), and a semiconductor substrate (fig. 3 indicator 14) being generally coincident with the longitudinal direction of the package (fig. 3.) It would have been obvious to one of ordinary skill in the art at the time of the invention to construct a package as taught by  
10   Hatta, with the image sensor as taught by the AAPA, so that the elongated semiconductor substrate of the line image sensor taught by the AAPA would be accommodated within the package.

          Hatta further teaches the lead electrodes extending from an end region of the elongated inner space (fig. 16 indicators 5 and 6.) It would have been obvious to one of  
15   ordinary skill in the art at the time of the invention to located the lead electrodes at the end regions as taught by Hatta, in order to coincide with the bonding pads, which are located outer than the photodiode group with respect to the longitudinal direction of the semiconductor substrate of the image sensor as taught by the AAPA, and therefore requiring the less wiring due to a shorter distance, as well as potentially less chance of  
20   requiring wires to cross.

          Hatta also teaches a light-suppressing layer which only allows light to pass through to an image area (fig. 1 and 2 indicator 7; col. 1 lines 24-33.) It would have

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been obvious to one of ordinary skill in the art at the time of the invention to include the light-suppressing layer to cover everywhere but where the light strikes the image area as taught by Hatta, with photodiodes of the image sensor as taught by the AAPA, in order to ensure the only light intended to strike the photodiode reaches the photodiode, as well as to prevent light from radiating to a part other than the imaging area.

Further, it is well known in the art to provide a peripheral circuit section formed on a semiconductor substrate and disposed outer than an image pickup section with respect to the longitudinal direction as demonstrated by Masuda (figs. 10 and 4a indicator 7.) It would have been obvious to one of ordinary skill in the art at the time of the invention to include circuitry peripheral to the photodiodes (figs. 10 and 4a indicator 4) and the charge transfer elements (figs. 10 and 4a indicator 5) as taught by Masuda, with the image sensor as taught by Hatta and the AAPA in order to minimize the width of the image sensor chip, resulting in a more compact image sensor, which is particularly important in full-page-width imaging.

Official Notice is taken regarding the etching of metal lines on a semiconductor substrate for the purposes of forming bonding pads, interconnects and trace runs; a practice that is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention for the image sensor as taught by Hatta, Masuda and the AAPA to include a plurality of metal lines formed on the surface of said semiconductor substrate, each of said metal lines having an end connected to one of said bonding pad and another end connected to the circuitry peripheral to the photodiodes in order to be able to pass signal from the photodiodes to the bonding pads

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and eventually to circuitry external to the semiconductor substrate for additional processing, such as to a printing apparatus, an image memory or an image display device.

Regarding claim 11, the AAPA, Hatta, Masuda, and Examiner' Official Notice

5 teach all the limitations of claim 11 (see the 103(a) rejection to claim 8 supra) including teaching an image sensor wherein said light-suppressing layer covers also said peripheral circuit section (figs. 1-3 indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents light from radiating to a part other than the imaging area.)

10 Regarding claim 12, the AAPA, Hatta, Masuda, and Examiner' Official Notice

teach all the limitations of claim 12 (see the 103(a) rejection to claim 8 supra) including teaching an image sensor wherein said light-suppressing layer covers said metal lines at least in a region sideward along said at least one photodiode group (figs. 1-3 indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents  
15 light from radiating to a part other than the imaging area.)

Regarding claim 17, the AAPA, Hatta, Masuda, and Examiner' Official Notice

teach all the limitations of claim 5 (see the 103(a) rejection to claim 1 supra) including teaching an image sensor chip wherein said light-suppressing layer covers said metal lines at least in a region sideward along said at least one photodiode group (figs. 1-3  
20 indicator 17; figs. 16 and 17 indicator 7; col. 1 lines 24-26; in which Hatta teaches the light shielding plate prevents light from radiating to a part other than the imaging area)

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and an edge portion of each of said bonding pads (figs. 1-3 indicators 15 and 17; figs. 16 and 17 indicators 4 and 7.)

**Claims 2, 3, 9, 10, 15 and 16** are rejected under 35 U.S.C. 103(a) as being  
5 unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hatta (US 5,087,964),  
in view of Masuda et al. (US 5,249,055), in view of Examiner's Official Notice, in further  
view of Miwada (US 5,220,210.)

Regarding claim 2, the AAPA, Hatta, Masuda, and Examiner' Official Notice  
teach all the limitations of claim 2 (see the 103(a) rejection to claim 1 supra) except for  
10 teaching an image sensor chip wherein all the bonding pads having an exposed surface  
are formed on the surface of said semiconductor substrate outer than said at least one  
photodiode group with respect to the longitudinal direction.

Nevertheless, Miwada is found to teach a similar linear image sensor in which  
the bonding pads are formed on the surface of said semiconductor substrate outer than  
15 said at least one photodiode group with respect to the longitudinal direction (figs. 1 and  
2 indicators a<sub>n</sub>; col. 2 line 65 – col. 3 line 2.) It would have been obvious to one of  
ordinary skill in the art at the time of the invention to combine the teachings of Miwada  
with the image sensor chip as taught in claim 1; in order to allow for further reduction in  
the width of the elongated substrate.

20 Regarding claim 3, the AAPA, Hatta, Masuda, and Examiner' Official Notice  
teach all the limitations of claim 3 (see the 103(a) rejection to claim 1 supra) except for

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teaching an image sensor chip wherein each of said bonding pads is disposed outer than said peripheral circuit section with respect to the longitudinal direction.

Nevertheless, Miwada is found to teach a similar linear image sensor in which the bonding pads are disposed outer than a circuit region with respect to the longitudinal direction (figs. 1 and 2 indicators  $a_n$ ; col. 2 line 65 – col. 3 line 2.) It would have been obvious to one of ordinary skill in the art at the time of the invention to locate the bonding pads outer a peripheral circuit section as taught by Miwada, with the configuration as taught in claim 1 in which the peripheral circuit section is disposed outer an image pickup section, with respect to the longitudinal direction, in order to allow for further reduction in the width of the elongated substrate.

Regarding claim 9, the AAPA, Hatta, Masuda, and Examiner' Official Notice teach all the limitations of claim 9 (see the 103(a) rejection to claim 8 supra) except for teaching an image sensor wherein all the bonding pads having exposed surfaces are formed on the surface of said semiconductor substrate outer than said at least one photodiode group with respect to the longitudinal direction of said semiconductor substrate.

Nevertheless, Miwada is found to teach a similar linear image sensor in which the bonding pads are formed on the surface of said semiconductor substrate outer than said at least one photodiode group with respect to the longitudinal direction of a semiconductor substrate (figs. 1 and 2 indicators  $a_n$ ; col. 2 line 65 – col. 3 line 2.) It would have been obvious to one of ordinary skill in the art at the time of the invention to

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combine the teachings of Miwada with the image sensor as taught in claim 1, in order to allow for further reduction in the width of the elongated substrate.

Regarding claim 10, the AAPA, Hatta, Masuda, and Examiner' Official Notice teach all the limitations of claim 10 (see the 103(a) rejection to claim 8 supra) except for  
5 teaching an image sensor wherein each of said bonding pads is disposed outer than said peripheral circuit section with respect to the longitudinal direction of said semiconductor substrate.

Nevertheless, Miwada is found to teach a similar linear image sensor in which the bonding pads are disposed outer than a circuit region with respect to the longitudinal  
10 direction of a semiconductor substrate (figs. 1 and 2 indicators  $a_n$ ; col. 2 line 65 – col. 3 line 2.) It would have been obvious to one of ordinary skill in the art at the time of the invention to locate the bonding pads outer a peripheral circuit section as taught by Miwada, with the configuration as taught in claim 1 in which the peripheral circuit section is disposed outer an image pickup section, with respect to the longitudinal direction, in  
15 order to allow for further reduction in the width of the elongated substrate.

Regarding claim 15, the AAPA, Hatta, Masuda, and Examiner' Official Notice teach all the limitations of claim 15 (see the 103(a) rejection to claim 8 supra) except for teaching an image sensor wherein each said lead electrode is disposed outer than said image pickup section with respect to the longitudinal direction of said semiconductor  
20 substrate.

Nevertheless, Miwada is found to teach lead electrodes being disposed outer than an image pickup section with respect to the longitudinal direction of the



semiconductor substrate (fig. 1 indicators 3-n.) It would have been obvious to one of ordinary skill in the art at the time of the invention to locate the lead electrodes outer than an image pickup section with respect to the longitudinal direction of the semiconductor substrate as taught by Miwada, with the image sensor as taught by the

5 AAPA, Hatta, Masuda, and Examiner' Official Notice, in order to further coincide with the bonding pads, which are located outer than the photodiode group with respect to the longitudinal direction of the semiconductor substrate of the image sensor as taught in claim 8, and therefore requiring even less wiring due to a shorter distance, as well as potentially less chance of requiring wires to cross.

10       Regarding claim 16, the AAPA, Hatta, Masuda, and Examiner' Official Notice teach all the limitations of claim 16 (see the 103(a) rejection to claim 8 supra) except for teaching an image sensor wherein each said lead electrode is disposed outer than said peripheral circuit section with respect to the longitudinal direction of said semiconductor substrate. However, it is further noted that Masuda is found to disclose the peripheral  
15 circuit section outer than the image pickup section with respect to the longitudinal direction (figs. 10 and 4a indicator 7), includes both the image pickup section and the peripheral circuit section on the same semiconductor substrate (fig. 10 indicator 3; col. 1 lines 27-39.)

      Miwada teaches the lead electrodes being disposed outer to the circuit region of  
20 the sensor chip with respect to the longitudinal direction of said semiconductor substrate (fig. 1, indicators 3, 2 and 10, respectively.) It would have been obvious to one of ordinary skill in the art at the time of the invention to locate the lead electrodes outer

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than the semiconductor substrate, with respect to the longitudinal direction as taught by Miwada, with the image sensor, which includes the peripheral circuit section as part of the semiconductor substrate, as taught by the AAPA, Hatta, Masuda, and Examiner' Official Notice, in order to further coincide with the bonding pads, which are located  
5 outer than the photodiode group and the peripheral circuit section with respect to the longitudinal direction of the semiconductor substrate of the image sensor as taught above, and therefore requiring even less wiring due to a shorter distance, as well as potentially less chance of requiring wires to cross.

10       **Claims 6 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hatta (US 5,087,964), in view of Masuda et al. (US 5,249,055), in view of Examiner's Official Notice, in further view of Kawai et al. (US 6,078,685), in further view of Phillips et al. (5,773,814.)

Regarding claim 6, the AAPA, Hatta, Masuda, and Examiner' Official Notice  
15 teach all the limitations of claim 6 (see the 103(a) rejection to claim 1 supra) except for teaching an image sensor chip wherein said image pickup section includes four photodiode groups juxtaposed along a direction crossing the longitudinal direction, said peripheral circuit section includes an output amplifier provided for each said charge transfer element and electrically connected to an output terminal of a corresponding  
20 charge transfer element, and the linear image sensor chip further comprises a color filter array disposed for each of three photodiode groups of said four photodiode groups,

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said color filter arrays generally constituting a multicolor color filter array necessary for taking a color image.

Nevertheless, Kawai is found to teach a plurality of light receiving units having a plurality of color filters, which include peripheral circuit sections that include output  
5 amplifiers for each charge transfer element and are electrically connected to an output terminal of the corresponding charge transfer element (figs. 2 and 3; col. 1 line 33 – col. 2 line 16.) It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kawai, with the linear image sensor chip as taught by the AAPA, Hatta, Masuda, and Examiner' Official Notice, in order to capture  
10 color images, while still attempting to minimize the width of the image sensor chip through placement of the peripheral circuit components.

Further, Phillips teaches an image sensor in which the image pickup section includes four sensor array groups juxtaposed along a direction crossing the longitudinal direction (fig. 6A and fig. 1 indicator 118), which also includes color filters disposed for  
15 three of the four sensor array groups, with the color filters generally constituting the multicolor color filter configuration necessary for taking a color image, and the fourth sensor array group not having a filter so that black and white or grayscale image capture can be performed (fig. 6A; col. 7 lines 7-38.) It would have been further obvious to one of ordinary skill in the art at the time of the invention to incorporate the four  
20 sensor array groups, with three of the four groups having color filters combinations necessary for taking a color image as taught by Phillips, with the linear image sensor chip as taught by the AAPA, Hatta, Masuda, Examiner' Official Notice and Kawai, so

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that the linear image sensor chip can be employed for black and white or grayscale image capture, in addition to the capture of color images.

Regarding claim 13, the AAPA, Hatta, Masuda, and Examiner' Official Notice teach all the limitations of claim 13 (see the 103(a) rejection to claim 8 supra) except for

5 teaching an image sensor wherein said image pickup section includes four photodiode groups juxtaposed along a direction crossing the longitudinal direction of said semiconductor substrate, said peripheral circuit section includes an output amplifier provided for each said charge transfer element and electrically connected to an output terminal of a corresponding charge transfer element, and said linear image sensor chip

10 further comprises a color filter array disposed for each of three photodiode groups of said four photodiode groups, said color filter arrays generally constituting a multicolor color filter array necessary for taking a color image.

Nevertheless, Kawai is found to teach a plurality of light receiving units having a plurality of color filters, which include peripheral circuit sections that include output

15 amplifiers for each charge transfer element and are electrically connected to an output terminal of the corresponding charge transfer element (figs. 2 and 3; col. 1 line 33 – col. 2 line16.) It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kawai, with the linear image sensor as taught by the AAPA, Hatta, Masuda, and Examiner' Official Notice, in order to capture color

20 images, while still attempting to minimize the width of the image sensor through placement of the peripheral circuit components.

Further, Phillips teaches an image sensor in which the image pickup section includes four sensor array groups juxtaposed along a direction crossing the longitudinal direction (fig. 6A and fig. 1 indicator 118), which also includes color filters disposed for three of the four sensor array groups, with the color filters generally constituting the  
5 multicolor color filter configuration necessary for taking a color image, and the fourth sensor array group not having a filter so that black and white or grayscale image capture can be performed (fig. 6A; col. 7 lines 7-38.) It would have been further obvious to one of ordinary skill in the art at the time of the invention to incorporate the four sensor array groups, with three of the four groups having color filters combinations  
10 necessary for taking a color image as taught by Phillips, with the linear image sensor as taught by the AAPA, Hatta, Masuda, Examiner' Official Notice and Kawai, so that the linear image sensor chip can be employed for black and white or grayscale image capture, in addition to the capture of color images.

15       **Claims 7 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hatta (US 5,087,964), in view of Masuda et al. (US 5,249,055), in view of Examiner's Official Notice, in view of Kawai et al. (US 6,078,685), in view of Phillips et al. (5,773,814), in further view of Sakamoto et al. (US 5,648,653.)

20       Regarding claim 7, the AAPA, Hatta, Masuda, Examiner' Official Notice, Kawai and Phillips teach all the limitations of claim 7 (see the 103(a) rejection to claim 6 supra)

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except for teaching an image sensor chip further comprising a color filter array disposed above remaining one of said four photodiode groups.

Nevertheless, Sakamoto teaches employing four color filters disposed above four image sensors groups, with the fourth filter converting infrared (figs. 1 and 2; col. 3 line 46 – col. 4 line 39.) It would have been obvious to one of ordinary skill in the art at the time of the invention to arrange four color filters above four image sensors groups as taught by Sakamoto, with the image sensor chip as taught by the AAPA, Hatta, Masuda, Examiner' Official Notice, Kawai and Phillips, so that the linear image sensor chip can be employed for color or black and white or grayscale image capture, in addition to the capture of images in the visible and invisible regions.

Regarding claim 14, the AAPA, Hatta, Masuda, Examiner' Official Notice, Kawai and Phillips teach all the limitations of claim 14 (see the 103(a) rejection to claim 13 supra) except for teaching an image sensor further comprising a color filter array disposed above remaining one of said four photodiode groups.

Nevertheless, Sakamoto teaches employing four color filters disposed above four image sensors groups, with the fourth filter converting infrared (figs. 1 and 2; col. 3 line 46 – col. 4 line 39.) It would have been obvious to one of ordinary skill in the art at the time of the invention to arrange four color filters above four image sensors groups as taught by Sakamoto, with the image sensor as taught by the AAPA, Hatta, Masuda, Examiner' Official Notice, Kawai and Phillips, so that the linear image sensor chip can be employed for color or black and white or grayscale image capture, in addition to the capture of images in the visible and invisible regions.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE  
5 MONTHS from the mailing date of this action. In the event a first reply is filed within  
TWO MONTHS of the mailing date of this final action and the advisory action is not  
mailed until after the end of the THREE-MONTH shortened statutory period, then the  
shortened statutory period will expire on the date the advisory action is mailed, and any  
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of  
10 the advisory action. In no event, however, will the statutory period for reply expire later  
than SIX MONTHS from the mailing date of this final action.

### ***Contact***

Any inquiry concerning this communication or earlier communications from the  
15 examiner should be directed to Gary C. Vieaux whose telephone number is 571-272-  
7318. The examiner can normally be reached on Monday - Friday, 8:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's  
supervisor, Thai Q. Tran can be reached on 571-272-7382. The fax phone number for  
the organization where this application or proceeding is assigned is 703-872-9306.

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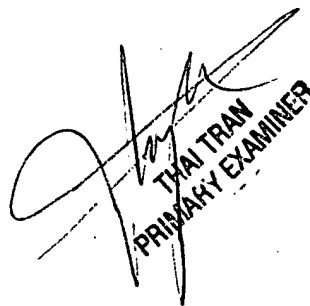
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

- 5 For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary C. Vieaux  
Examiner  
Art Unit 2612

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Gcv2

  
THAI TRAN  
PRIMARY EXAMINER